REMARKS

Claims 1-6, 8-13, 5 and 20-23 are pending in the application. Claims 1-6 are withdrawn from consideration and claims 9, 15, 21 and 22 are amended.

Claim Rejections under 35 USC §112

Claims 21 and 22 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically claims 21 and 22 are rejected for failing to indicate what "W1" and "L1" correspond to in the structure of the claimed invention. Claims 21 and 22 have been amended to indicate that "W1 corresponds to the width of the wiring part, L1 corresponds to the width of the first width" defined in claim 9. Therefore withdrawal of the rejection of claims 21 and 22 under 35 U.S.C. §112, second paragraph, is respectfully requested.

Claim Rejections under 35 USC §103

Claims 8-13 and 15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Harada et al. in view of Lee et al. (U.S. 6,163,074).

The present invention is a semiconductor device having a pad capable of suppressing excess current concentration. As illustrated in Fig. 2a, the pad includes a large number of insulating regions (21a) in which specific ratios of dimensions are followed. For example, W1 corresponds to the

width of the wiring portion (25). The pad is divided into three portions. A first frame area (27a) having a width of L1. A second frame area (27c) has a width L2 and contains several insulating regions (21a). A central area (27d) is contained in the middle of the pad and may contain a via hole. The width L1 of the first frame area (27 a) is equal to or wider than the distance between insulating regions (21a). As illustrated in Fig. 2A, the total width of pad (27) corresponds to 2 x W2 + n x W3 as discussed on page 11, line 22 of the specification, W1 correspond to the distance L1 and W3 corresponds to the distance P2. As discussed in the example provided on page 12, lines 4-11, W1 is larger than the distance L1 and the ratio L1/W1 is 30 percent or higher.

Lee et al. describes a semiconductor device having a lower single-bodied conductive plug (930) and a lower island insulator (925I) as shown in figures 9 and 10. With this design a bonding pad having reduced cracking in an insulating layer is possible.

Harada et al. describes a semiconductor device and method of manufacturing the same which includes a pad electrode and main electrode layer. This device includes a first interlayer insulating film (7) a first intra-layer insulating film (11).

In Harada's device, the upper surface of the insulating region (341) is on a level with the upper surface of the layer (230c), the upper surface of the pad (250) is on a level with the upper surface of the layer (230d), and he upper surface of the wiring that is continued to the pad (101) as shown in Fig. 77A is on a level with the upper surface of the layer (15d). Namely, the upper surfaces of the insulating regions, the pad and the wiring are not on the same level as recited in amended claim 9 of the present application.

In Harada's device, as shown in Figs. 77A to 77C, the wiring is continued to the pad (101). The insulating regions (341) do not prevent current from flowing from the wiring into the pad (101) because the insulating regions (341) are disposed at the level different from the wiring and the pad (101). In contrast, the claim 9, the insulating regions could prevent current from flowing from the wiring into the pad. It averts interruption of the current flow that the insulating regions are not disposed in the near wiring area.

As described above, the current flow paths are different between the invention of claim 9 and Harada's invention.

Therefore, claim 9 patentably distinguishes over the prior art relied upon by reciting,

> "A semiconductor device comprising: a semiconductor substrate; a first interlayer insulating film made of insulating material and formed on the semiconductor substrate; a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part, a plurality of insulating regions disposed on the bottom of the pad part, and the recess being formed so that the insulating regions are not disposed in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width but disposed in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width; a first pad filled in the pad part of the recess; and a wiring filled in the wiring part of the recess, wherein upper surfaces of said first pad, said wiring and said insulating regions are on a same level." (Emphasis Added)

Regarding claim 15, the claim has been amended so as to include the limitation that upper surfaces of the first pad and the insulating regions are on the same level. The prior art of record fails

to describe this limitation. The advantageous effect of claim 15 is when the wire is bonded to the pad, the pad becomes stressed. The stress is easy to concentrate to the periphery region (the first frame are) of the pad. The pad recited in claim 15 can withstand the stress concentration because the recess area of the first frame area is large. Therefore, claim 15 patentably distinguishes over the prior art of record by reciting,

> "A semiconductor device comprising: a semiconductor substrate; a first interlayer insulating film made of insulating material and formed on the semiconductor substrate; a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part, a plurality of insulating regions disposed on the bottom of the pad part, and the recess being formed so that the insulating regions are not disposed in a first frame area having as an outer periphery an outer periphery of the pad part and having a first width but disposed in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width; and a first pad filled in the pad part of the recess, wherein upper surfaces of said first pad and said insulating regions are on a same level." (Emphasis Added)

Therefore, withdrawal of the rejection of claims 8-13 and 15 under 35 U.S.C. §103(a) as being unpatentable over Harada et al. in view of Lee et al. (U.S. 6,163,074) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 9, 15, 21 and 22, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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